
PAN3201DH LOW POWER CMOS OPTICAL MOUSE SENSOR

General Description

The PAN3201DH is a high performance and low power CMOS process optical mouse sensor with DSP integration chip that serves as a non-mechanical motion estimation engine for implementing a computer mouse.

Features

- Single power supply
- Precise optical motion estimation technology
- Complete 2-D motion sensor
- No mechanical parts
- Accurate motion estimation over a wide range of surfaces
- High speed motion detection up to 37 inches/sec
- High resolution up to 1000dpi
- Resolution setting by two method
 - ◇ CPI IO trap select pin (pin15) to 400, 600, 800 dpi
 - ◇ Register setting to 400, 500, 600, 800, 1000 dpi
- Power down pin and register setting for low power dissipation.
- Power saving mode during times of no movement
- Serial Interface for programming and data transfer
- SWKINT pin to wake up micro-controller when sensor wakeup from sleep mode

Key Specification

Power Supply	1.73V~1.87V (VDDD,VDDA, VDD) 2.5V~2.9V (VDD)
Optical Lens	1:1
System Clock	18.432 MHz
Speed	37 inches/sec @ F _{CLK} =24.576MHz
Resolution	400/500/600/800(default)/1000 dpi
Frame Rate	3000 frames/sec
Operating Current	4.5mA @Mouse moving (Normal) 600uA @Mouse not moving (Sleep1) 100uA @Mouse not moving (Sleep2) 30uA @Power down mode
Package	Shrunk DIP20

Ordering Information

Order number	I/O	Resolution
PAN3201DH	CMOS output	800 dpi

1. Pin Description

Pin No.	Name	Type	Definition
1	VSS_LED	GND	LED ground
2	LED	OUT	LED control
3	OSCOUT	OUT	Resonator output
4	OSCIN	IN	Resonator input
5	VDDD	PWR	Chip digital power, 1.8V
6	VSSD	GND	Chip digital ground
7	VSSA	GND	Chip analog ground
8	VDD	PWR	Chip I/O power voltage, 1.73V~1.87V(V_{dd1}) or 2.5V~2.9V(V_{dd2})
9	VDDA	PWR	Chip analog power, 1.8V
10	VREF	BYPASS	Analog voltage reference
11	YA	OUT	YA quadrature output
12	YB	OUT	YB quadrature output
13	XA	OUT	XA quadrature output
14	XB	OUT	XB quadrature output
15	CPI	IN	CPI IO trap select pin Pull-high to VCC (V_{dd1} or V_{dd2}) : 600 cpi Pull-low to GND : 800 cpi Floating : 400 cpi
16	NC	-	No connection
17	SWKINT	OUT	Sensor wakeup interrupt
18	SCLK	IN	Serial interface clock
19	SDIO	I/O	Serial interface bi-direction data
20	PD	IN	Power down pin, active high

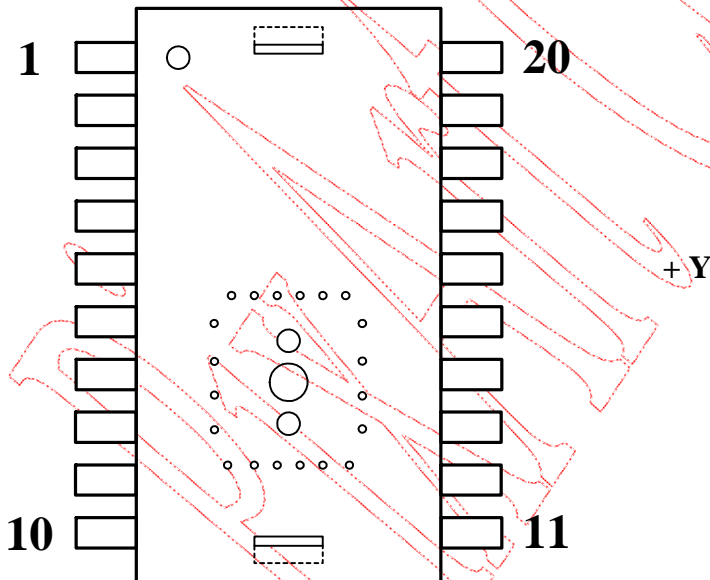


Figure 1. Top view pinout

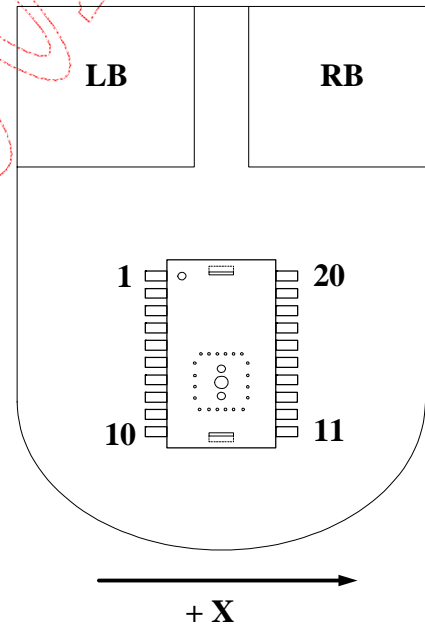


Figure 2. Top view of mouse

2. Block Diagram and Operation

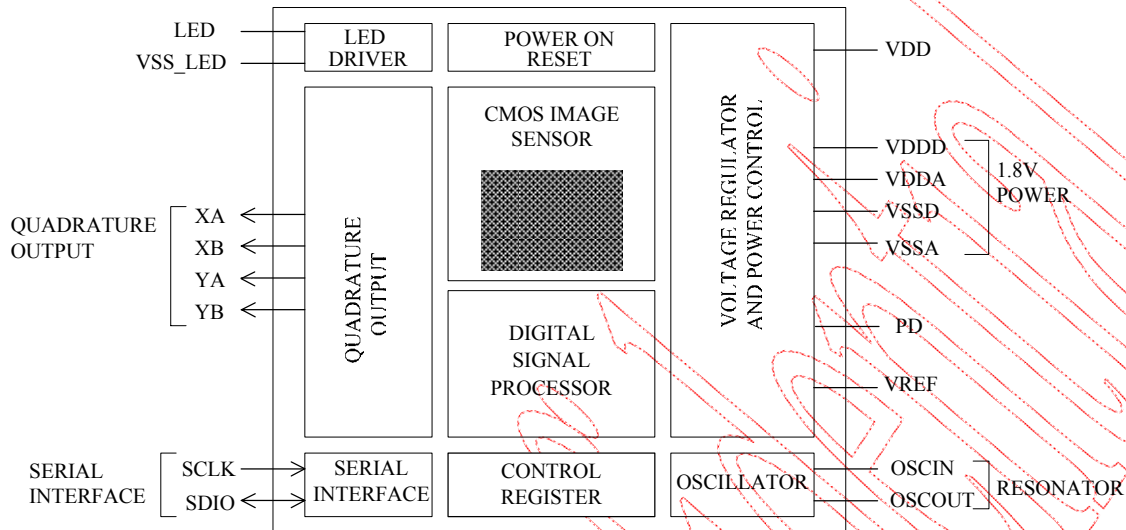


Figure3. Block diagram

The PAN3201DH is a high performance and low power CMOS-process optical mouse sensor with DSP integration chip that serves as a non-mechanical motion estimation engine for implementing a computer mouse. It is based on new optical navigation technology, which measures changes in position by optically acquiring sequential surface images (frames) and mathematically determining the direction and magnitude of movement. The sensor is in a 20pin optical package. The output format is two-channel quadrature (X and Y direction), which emulates encoder phototransistors. The current X and Y information are also available in registers accessed via a serial port.

3. Registers and Operation

The PAN3201DH can be programmed through registers, via the serial port, and DSP configuration and motion data can be read from these registers. All registers not listed are reserved, and should never be written by firmware.

3.1 Registers

Address	Name	R/W	Default	Data Type
0x00	Product_ID	R	0x30	Eight bits [11:4] number with the product identifier
0x01	Product_ID	R	0x2N	Four bits [3:0] number with the product identifier Reserved [3:0] number is reserved for future
0x02	Motion_Status	R	-	Bit field
0x03	Delta_X	R	-	Eight bits 2's complement number
0x04	Delta_Y	R	-	Eight bits 2's complement number
0x05	Operation_Mode	R/W	-	Bit field
0x06	Configuration	R/W	-	Bit field
0x07	Image_Quality	R	-	Eight bits unsigned integer

3.2 Register Descriptions

0x00	Product_ID							
Bit	7	6	5	4	3	2	1	0
Field	PID[11:4]							
Usage	The value in this register can't change. It can be used to verify that the serial communications link is OK.							
0x01	Product_ID							
Bit	7	6	5	4	3	2	1	0
Field	PID[3:0]				Reserved [3:0]			
Usage	The value in this register can't change. PID[3:0] can be used to verify that the serial communications link is OK. Reserved [3:0] is a value between 0x0 and 0xF, it can't be used to verify that the serial communications.							

0x02	Motion_Status							
Bit	7	6	5	4	3	2	1	0
Field	Motion	Reserved[6:5]		DYOVF	DXOVF	RES[2:0]		
Usage	<p>Register 0x02 allows the user to determine if motion has occurred since the last time it was read. If so, then the user should read registers 0x03 and 0x04 to get the accumulated motion. It also tells if the motion buffers have overflowed since the last reading. The current resolution is also shown.</p> <p>Reading this register freezes the Delta_X and Delta_Y register values. Read this register before reading the Delta_X and Delta_Y registers. If Delta_X and Delta_Y are not read before the motion register is read a second time, the data in Delta_X and Delta_Y will be lost.</p>							
Notes	Field Name	Description						
	Motion	Motion since last report or PD 0 = No motion (Default) 1 = Motion occurred, data ready for reading in Delta_X and Delta_Y registers						
	Reserved[6:5]	Reserved for future						
	DYOVF	Motion Delta Y overflow, ΔY buffer has overflowed since last report 0 = No overflow (Default) 1 = Overflow has occurred						
	DXOVF	Motion Delta X overflow, ΔX buffer has overflowed since last report 0 = No overflow (Default) 1 = Overflow has occurred						
	RES[2:0]	Resolution in counts per inch 000 = 400 001 = 500 010 = 600 011 = 800 100 = 1000						
0x03	Delta_X							
Bit	7	6	5	4	3	2	1	0
Field	X7	X6	X5	X4	X3	X2	X1	X0
Usage	X movement is counts since last report. Absolute value is determined by resolution. Reading clears the register. Report range -128~+127.							
0x04	Delta_Y							
Bit	7	6	5	4	3	2	1	0
Field	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0
Usage	Y movement is counts since last report. Absolute value is determined by resolution. Reading clears the register. Report range -128~+127.							

0x05	Operation_Mode																									
Bit	7	6	5	4	3	2	1	0																		
Field	LEDsht_enh	XY_enh	Reserved	Slp_enh	Slp2au	Slp2mu	Slp1mu	Wakeup																		
Usage	<p>Register 0x05 allows the user to change the operation of the sensor. Shown below are the bits, their default values, and optional values.</p> <p>Operation_Mode[4:0] “0xxx”=Disable sleep mode “10xxx”=Enable sleep mode¹ “11xxx”=Enable sleep mode² “1x100”=Force enter sleep2³ “1x010”=Force enter sleep1³ “1x001”=Force wakeup from sleep mode³</p> <p>Notes: 1. Enable sleep mode, but disable automatic entering sleep2 mode, that is, only 2 modes will be used, normal mode and sleep1 mode. After 200 ms not moving during normal mode, the chip will enter sleep1 mode, and keep on sleep1 mode until moving is detected or wakeup is asserted. 2. Enable sleep mode full function, that is 3 modes will be used, normal mode, sleep1 mode and sleep2 mode. After 200 ms not moving during normal mode, chip will enter sleep1 mode, and keep on sleep1 mode until moving is detected or wakeup is asserted. And after 30 sec not moving during sleep1 mode, the chip will enter sleep2 mode, and keep on sleep2 mode until detect moving or force wakeup to normal mode.</p> <table border="1"> <thead> <tr> <th>Mode</th> <th>Sampling rate @3000frame/sec</th> <th>Active duty cycle @3000frame/sec</th> </tr> </thead> <tbody> <tr> <td>Sleep1</td> <td>77/sec</td> <td>3.8%</td> </tr> <tr> <td>Sleep2</td> <td>8/sec</td> <td>0.4%</td> </tr> </tbody> </table> <p>3. Only one of these three bits slp2mu_enh, slp1mu_enh, and wakeup can be set to 1 at the same time, others have to be set to 0. After a period of time, the bits, which was set to 1, will be reset to 0 by internal signal.</p>								Mode	Sampling rate @3000frame/sec	Active duty cycle @3000frame/sec	Sleep1	77/sec	3.8%	Sleep2	8/sec	0.4%									
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Slp1mu	Manual enter sleep1 mode, set “1” will enter sleep2 and this bit will be reset to “0”																									
Wakeup	Manual wake up from sleep mode, set “1” will enter wakeup and this bit will be reset to “0”																									

0x06	Configuration							
Bit	7	6	5	4	3	2	1	0
Field	Reset	Reserved	Cpimd	Swk_enh	PD	Reserved	CPI [1:0]	
Usage	The Configuration register allows the user to change the configuration of the sensor. Shown below are the bits, their default values, and optional values.							
Notes	Field Name	Description						
	Reset	Full chip reset 0 = Normal operation mode (Default) 1 = Full chip reset						
	Reserved[7:4]	Reserved for future						
	Cpimd	Cpi mode select						
	PD	Power down mode 0 = Normal operation (Default) 1 = Power down mode						
	Reserved	Reserved for future						
	CPI[1:0]	Output resolution setting, setting with cpi mode select bit (Cpimd) Cpimd = 0 00 = 800 01 = 400 10 = 400 11 = 600 Cpimd = 1 00 = 1000 01 = 500 10 = 500 11 = 800						
0x07	Image_Quality							
Bit	7	6	5	4	3	2	1	0
Field	Imgqa[7:0]							
Usage	Image Quality is a quality level of the sensor in the current frame. Report range 0~255. The minimum level for normally working is 15.							
Notes	Field Name	Description						
	Imgqa[7:0]	Image quality report range: 0(worst) ~ 255(best).						

4. Specifications

Absolute Maximum Ratings

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Symbol	Parameter	Min	Max	Unit	Notes
T _{STG}	Storage temperature	-40	85	°C	
T _A	Operating Temperature	-15	55	°C	
V _{DC}	DC supply voltage	-0.5	V _{dd1} + 0.2	V	
		-0.5	V _{dd2} + 0.3	V	
V _{IN}	DC input voltage	-0.5	V _{DC}	V	All I/O pin
	Lead Solder Temp	-	260	°C	For 10 seconds, 1.6mm below seating plane.
ESD		-	2	kV	All pins, human body model MIL 883 Method 3015

Recommend Operating Condition

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
T _A	Operating Temperature	0	-	40	°C	
V _{dd1}	Power supply voltage	1.73	1.8	1.87	V	VDDD, VDDB, VDD short
V _{dd2}		2.5	2.7	2.9		VDD
V _N	Supply noise	-	-	100	mV	Peak to peak within 0-100 MHz
Z	Distance from lens reference plane to surface	2.3	2.4	2.5	mm	Refer to Figure 4.
R	Resolution	400	800	1000	cpi	
A	Acceleration	-	-	TBD	g	
SCLK	Serial Port Clock Frequency	-	-	10	MHz	
C _L	Load capacitance of resonator	15	-	30	pF	15 pF @ F _{CLK} =24.567MHz 30 pF @ F _{CLK} =18.432MHz
F _{CLK}	Clock Frequency	12.000	18.432	24.576	MHz	Set by crystal or ceramic resonator.
FR	Frame Rate	1953	3000	4000	Frames/s	1953 frames/s @ F _{CLK} =12.000MHz 3000 frames/s @ F _{CLK} =18.432MHz 4000 frames/s @ F _{CLK} =24.567MHz
S	Speed	18	28	37	Inches/s	18 inches/s @ F _{CLK} =12.000MHz 28 inches/s @ F _{CLK} =18.432MHz 37 inches/s @ F _{CLK} =24.567MHz

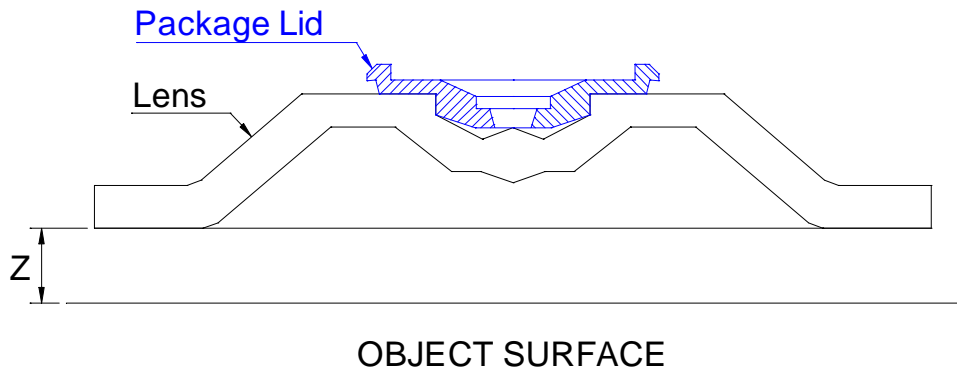


Figure4. Distance from Lens Reference Plane to Surface

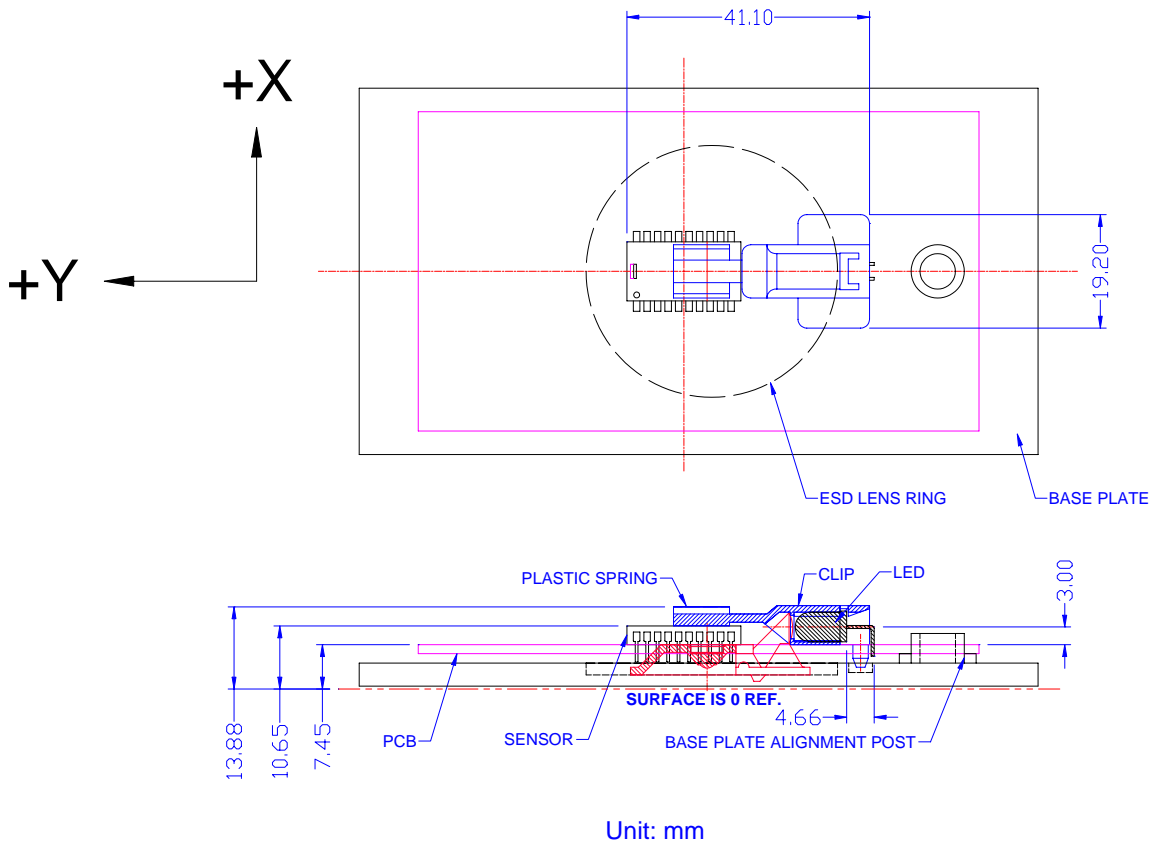


Figure5. 2D assembly

AC Operating Condition

Electrical Characteristics over recommended operating conditions. Typical values at 25 °C, $V_{DD}=1.8$ V, pin 5,8,9 short, $F_{CLK}=18.432$ MHz

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
t_{PDR}	PD Pulse Register	-	-	333	us	One frame time maximum after setting bit 3 in the Configuration register @3000frame/sec. (Refer to Figure 16)
t_{PD}	Power Down	-	500	-	us	From PD \uparrow . (Refer to Figure 14)
t_{PDW}	PD Pulse Width	700	-	-	us	Pulse width to reset the serial interface. (Refer to Figure 14)
t_{PUPD}	Power Up from PD \downarrow	TBD	-	TBD	ms	From PD \downarrow to valid quad signals. After t_{PUPD} , all registers contain valid data from first image after PD \downarrow . Note that an additional TBD frames for Auto-Exposure (AE) stabilization may be required if mouse movement occurred while PD was high. (Refer to Figure 14)
t_{PU}	Power Up from $V_{DD}\uparrow$	TBD	-	TBD	ms	From $V_{DD}\uparrow$ to valid quad signals. 500usec + TBD frames.
t_{HOLD}	SDIO read hold time	-	3	-	us	Minimum hold time for valid data. (Refer to Figure 11)
t_{RESYNC}	Serial Interface RESYNC	1	-	-	us	@3000frame/sec (Refer to Figure 13)
t_{SIWTT}	Serial Interface Watchdog Timer Timeout	1.7	-	-	ms	@3000frame/sec (Refer to Figure 13)
t_{SWKINT}	Sensor wakeup interrupt time	160	333	-	us	
t_r, t_f	Rise and Fall Times: SDIO	-	25, 20	-	ns	$C_L = 30$ pf
t_r, t_f	Rise and Fall Times: XA, XB, YA, YB	-	30, 25	-	ns	$C_L = 30$ pf
t_r, t_f	Rise and Fall Times: ILED	-	10, 10	-	ns	LED bin grade: R; R1=100ohm

DC Electrical Characteristics

Electrical Characteristics over recommended operating conditions. Typical values at 25 °C, V_{DD} =1.8 V, pin 5,8,9 short, F_{CLK}=18.432MHz

Symbol	Parameter	Min.	Typ.	Max.	Unit	
Type: Power						
I _{DD}	Supply Current Mouse moving (Normal)		4.5		mA	
I _{DD}	Supply Current Mouse not moving (sleep1)		600		uA	
I _{DD}	Supply Current Mouse not moving (Sleep2)		100		uA	PD, SCLK, SDIO = high
I _{DDPD}	Supply Current (Power Down)		30		uA	
Type: SCLK, SDIO, PD						
V _{IH}	Input voltage HIGH	1.25				
V _{IL}	Input voltage LOW			0.5	V	
Type: LED						
V _{OL}	Output voltage LOW			300	mV	@I _{OL} = 25mA
Type: XA, XB, YA, YB						
V _{OH}	Output voltage HIGH	1.2			V	@I _{OH} = 2mA
V _{OL}	Output voltage LOW			0.2	V	@I _{OL} = 2mA

5. Quadrature Mode

The quadrature state of the PAN3201DH tells mouse controller which direction the mouse is moving in. The output format is two channels quadrature (X and Y direction), which emulates encoder phototransistors. The DSP generates the Δx and Δy relative displacement values that are converted into two channel quadrature signals. The following diagrams show the timing for positive X motion, to the right or positive Y motion, up.

5.1 Quadrature Output Timing

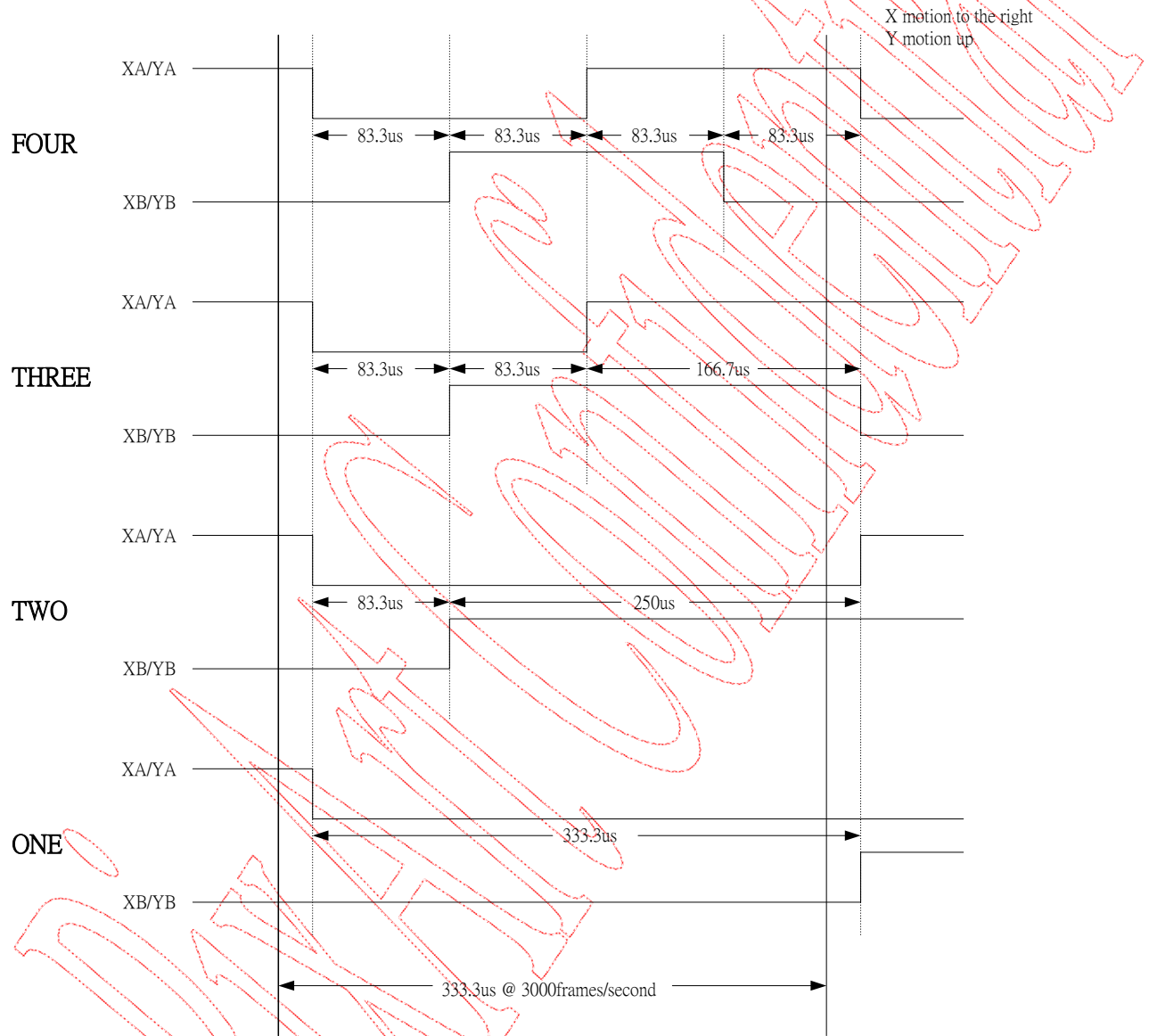


Figure6. Quadrature output timing

5.2 Quadrature Output State Machine

The following state machine shows the states of the quadrature output pins. The three things to note are that state 0 is entered after a power on reset. While the PD pin is asserted, the state machine is halted. Once PD is deasserted, the state machine picks up from where it left off. During times of mouse no movement will entry power saving mode, until mouse was moved.

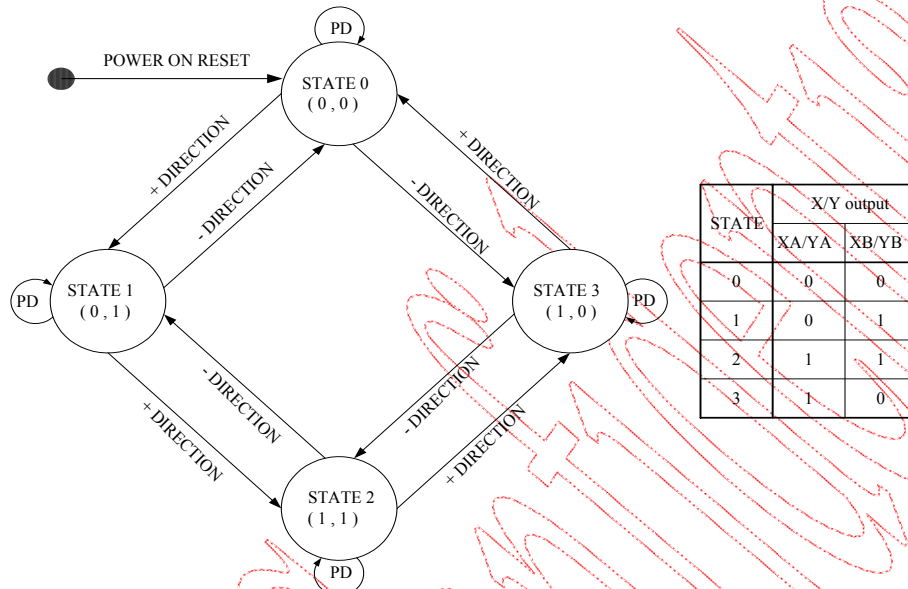


Figure7. State machin

5.3 Quadrature Output Waveform

The following diagrams show the waveform of the two channel quadrature outputs. If the X, Y is motionless, the (XA, XB), (YA, YB) will keep in final state. Each state change (ex. STATE2 → STATE3) is one count.

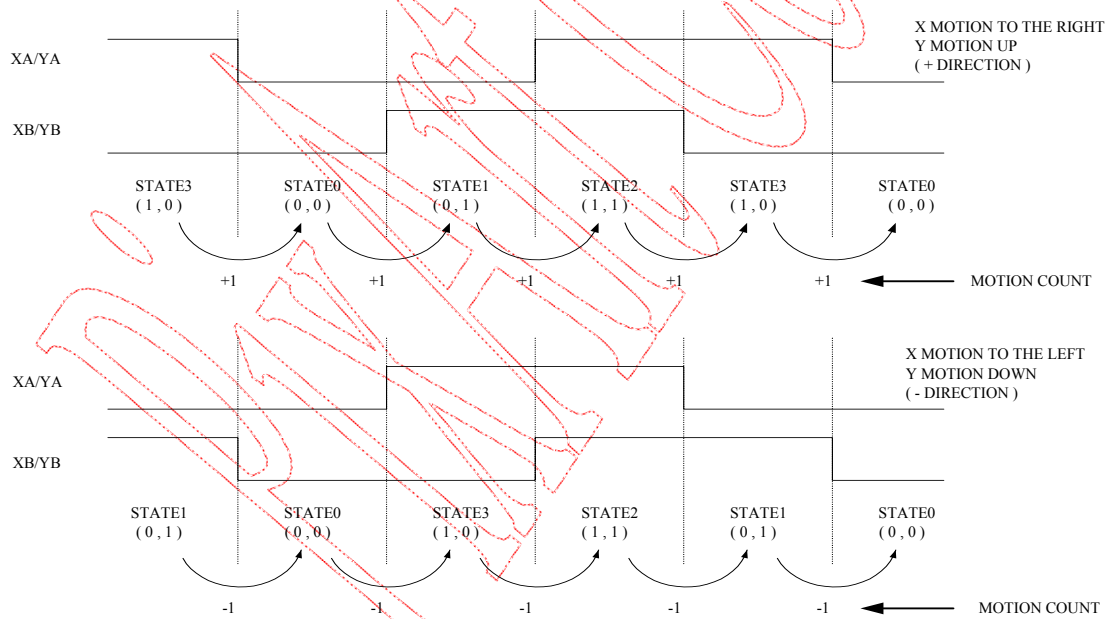


Figure8. Quadrature output waveform

6. Serial Interface

The synchronous serial port is used to set and read parameters in the PAN3201DH, and can be used to read out the motion information instead of the quadrature data pins.

SCLK: The serial clock line. It is always generated by the host micro-controller.

SDIO: The serial data line used for write and read data.

PD: A third line is sometimes involved. PD(Power Down pin) is usually used to place the PAN3201DH in a low power mode to meet USB suspend specification. PD can also be used to force re-synchronization between the micro-controller and the PAN3201DH in case of an error.

6.1 Transmission Protocol

The transmission protocol is a two-wire link, half duplex protocol between the micro-controller and PAN3201DH. All data changes on SDIO are initiated by the falling edge on SCLK. The host micro-controller always initiates communication; the PAN3201DH never initiates data transfers.

The transmission protocol consists of the two operation modes:

- Write Operation.
- Read Operation.

Both of the two operation modes consist of two bytes. The first byte contains the address (seven bits) and has a bit7 as its MSB to indicate data direction. The second byte contains the data.

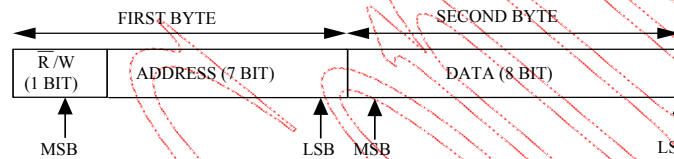


Figure9. Transmission Protocol

6.1.1 Write Operation

A write operation, which means that data is going from the micro-controller to the PAN3201DH, is always initiated by the micro-controller and consists of two bytes. The first byte contains the address (seven bits) and has a “1” as its MSB to indicate data direction. The second byte contains the data. The transfer is synchronized by SCLK. The micro-controller changes SDIO on falling edges of SCLK. The PAN3201DH reads SDIO on rising edges of SCLK.

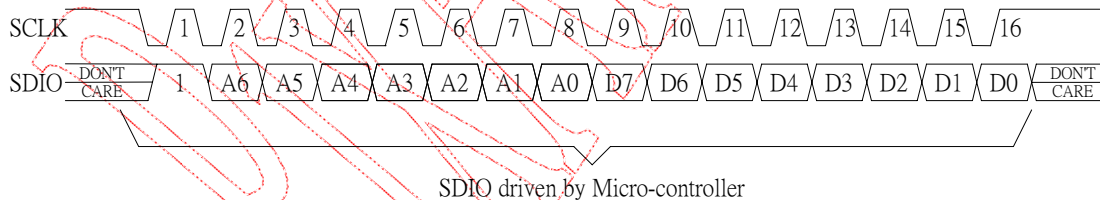


Figure10. Write Operation

6.1.2 Read Operation

A read operation, which means that data is going from the PAN3201DH to the micro-controller, is always initiated by the micro-controller and consists of two bytes. The first byte contains the address, is written by the micro-controller, and has a "0" as its MSB to indicate data direction. The second byte contains the data and is driven by the PAN3201DH. The transfer is synchronized by SCLK. SDIO is changed on falling edges of SCLK and read on every rising edge of SCLK. The micro-controller must go to a high Z state after the last address data bit. The PAN3201DH will go to the high Z state after the last data bit.

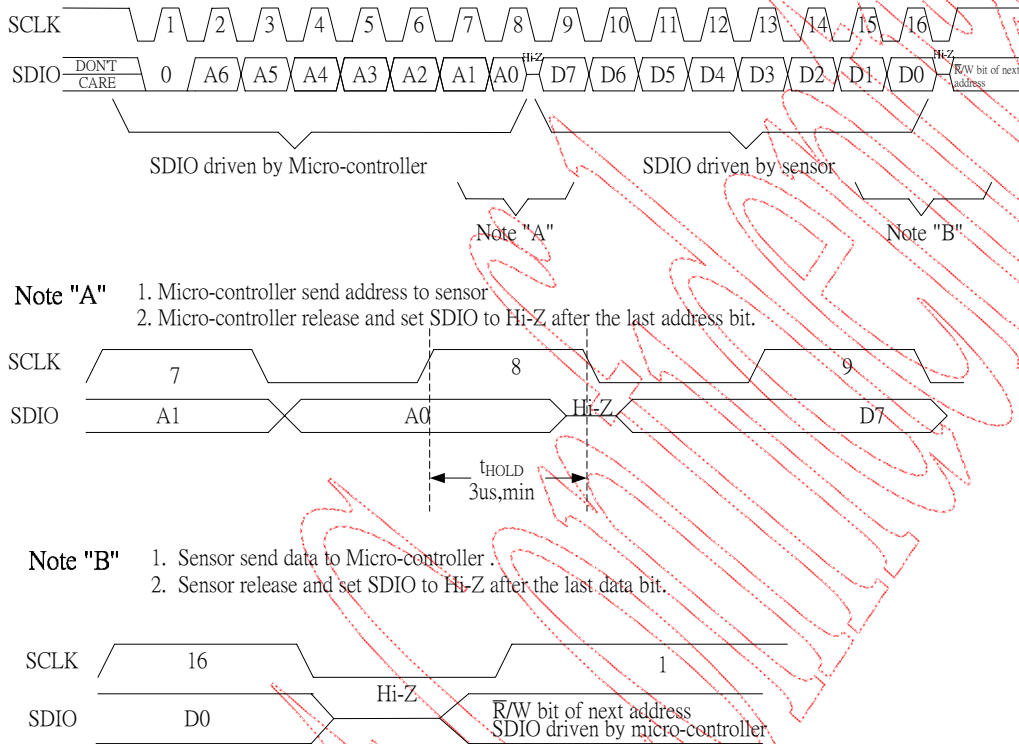


Figure11. Read Operation

6.2 Re-Synchronous Serial Interface

There are times when the SDIO line from the PAN3201DH should be in the Hi-Z state. If the microprocessor has completed a write to the PAN3201DH, the SDIO line is Hi-Z, since the SDIO pin is still configured as an input. However, if the last operation from the microprocessor was a read, the PAN3201DH will hold the D0 state on SDIO until a rising edge of SCLK. To place the SDIO pin into the Hi-Z state, first raise the PD line, and then toggle the SCLK line from high to low to high. The SDIO line will now be in the Hi-Z state. The PAN3201DH and the micro-controller might get out of synchronization due to following condition.

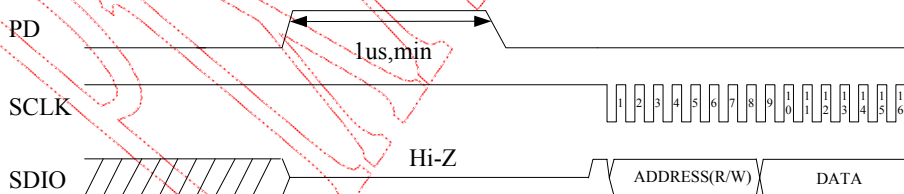


Figure12. Forcing PAN3201DH SDIO line to the Hi-Z stat

6.2.1 USB Suspend

Termination of a transmission by the micro-controller may sometimes be required (for example, due to a USB suspend interrupt during a read operation). To accomplish this, the micro-controller should raise PD. The PAN3201DH will not write to any register and will reset the serial port (but nothing else) and be prepared for the beginning of future transmissions after PD goes low.

6.2.2 Firmware Flaws Error, or Others Error

The PAN3201DH and the micro-controller might get out of synchronization due to micro-controller firmware flaws. The PD pin can stay high, with the PAN3201DH in the shutdown state, or the PD pin can be lowered, returning the PAN3201DH to normal operation.

If the microprocessor and the PAN3201DH get out of sync, then the data either written or read from the registers will be incorrect. In such a case, an easy way to solve this is to raise PD to re-sync the parts after an incorrect read. The PAN3201DH will reset the serial port but will not reset the registers and be prepared for the beginning of a new transmission.

6.2.3 Power On Problem

The problem occurs if the PAN3201DH powers up before the microprocessor sets the SCLK and SDIO lines to be output.

6.3 Collision Detection on SDIO

The only time that the PAN3201DH drives the SDIO line is during a READ operation. To avoid data collisions, the micro-controller should release SDIO before the falling edge of SCLK after the last address bit. The PAN3201DH begins to drive SDIO after the next falling edge of SCLK. The PAN3201DH release SDIO of the rising SCLK edge after the last data bit. The micro-controller can begin driving SDIO any time after that. In order to maintain low power consumption in normal operation or when the PD pin is pulled high, the micro-controller should not leave SDIO floating until the next transmission (although that will not cause any communication difficulties).

6.4 Serial Interface Watchdog Timer Timeout

When there are only two pins to read register from PAN3201DH, and PD pin can't be used to re-synchronous function. If the microprocessor and the PAN3201DH get out of sync, then the data either written or read from the registers will be incorrect. In such a case, an easy way to solve this condition is to toggle the SCLK line from high to low to high and wait at least t_{SIWTT} to re-sync the parts after an incorrect read. The PAN3201DH will reset the serial port but will not reset the registers and be prepared for the beginning of a new transmission.

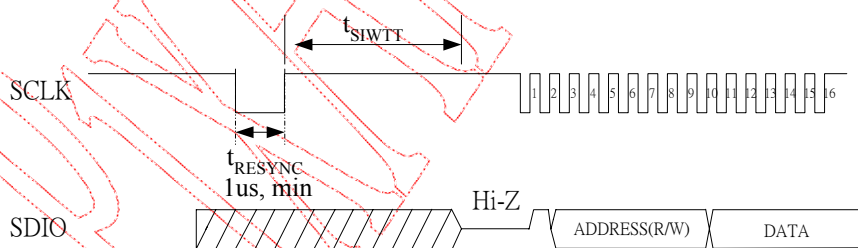


Figure13. Re-synchronous serial interface using watchdog timer timeout

6.5 Power Down Mode

There are two different ways to entry power down mode, using the PD line or register setting.

6.5.1 PD Line Power Down Mode

To place the PAN3201DH in a low power mode to meet USB suspend specification, raise the PD line at least 700us. Then PD line can stay high, with the PAN3201DH in the shutdown state, or the PD pin can be lowered, returning the PAN3201DH to normal operation.

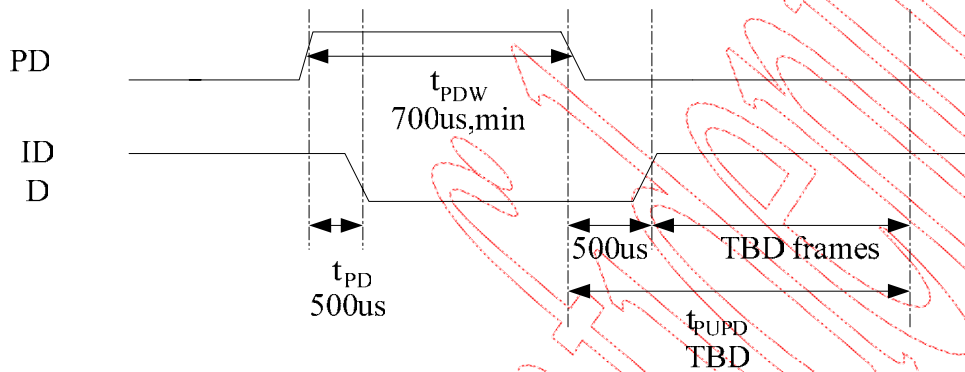


Figure14. Power Down Minimum Pulse Width

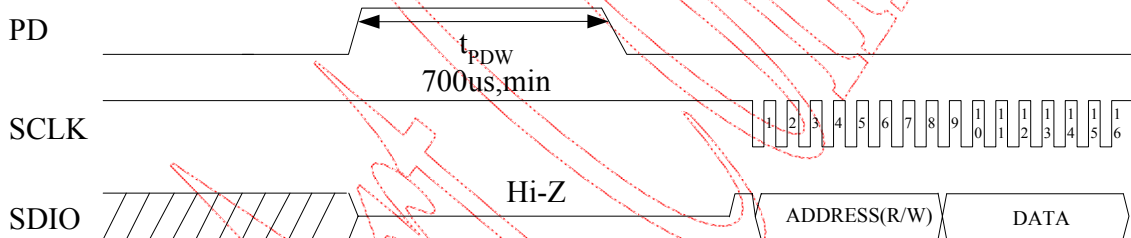


Figure15. PD Line Power Down Mode

6.5.2 Register Power Down Mode

PAN3201DH can be placed in a power-down mode by setting bit 3 in the configuration register via a serial port write operation. After setting the configuration register, wait at least 1 frame times. To get the chip out of the power-down mode, clear bit 3 in the configuration register via a serial port write operation. In power-down mode, the serial interface watchdog timer is not available. But, The serial interface still can read/write normally. For an accurate report after leave power down mode, wait about 3ms before the micro-controller is able to issue any write/read operation to the PAN3201DH.

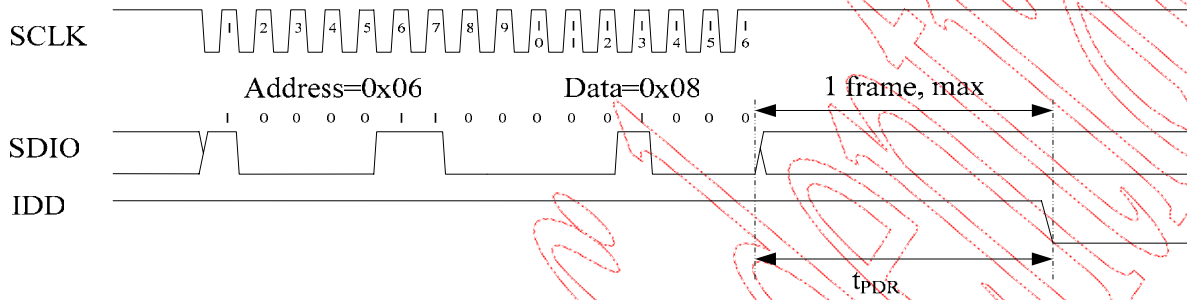


Figure16. Power-down configuration register writing operation

6.6 Error Detection

1. The micro-controller can verify success of write operations by issuing a read command to the same address and comparing written data to read data.
2. The micro-controller can verify the synchronization of the serial port by periodically reading the product ID register

7. SWKINT Timing

When the PAN3201DH is in sleep mode and the micro-controller is also in sleep mode, if the PAN3201DH finds motion occurred at this moment, PAN3201DH will wake micro-controller up promptly via SWKINT.

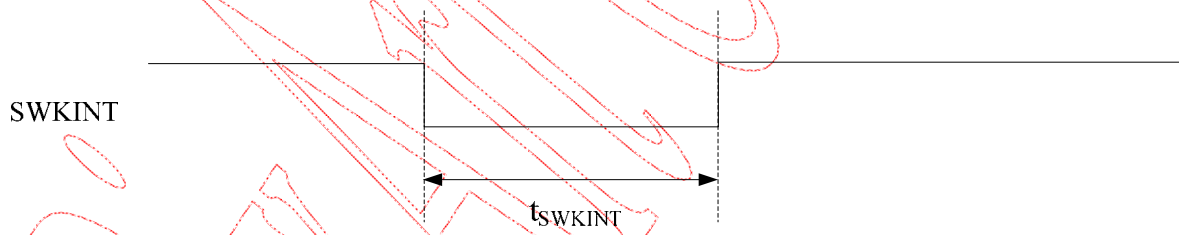


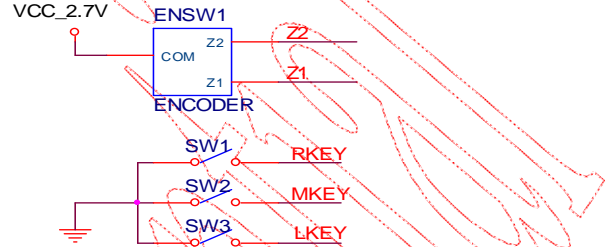
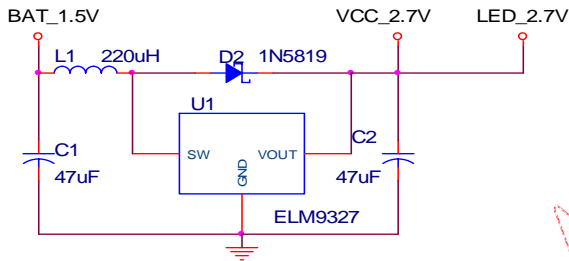
Figure13. SWKINT Timing

8. Referencing Application Circuit

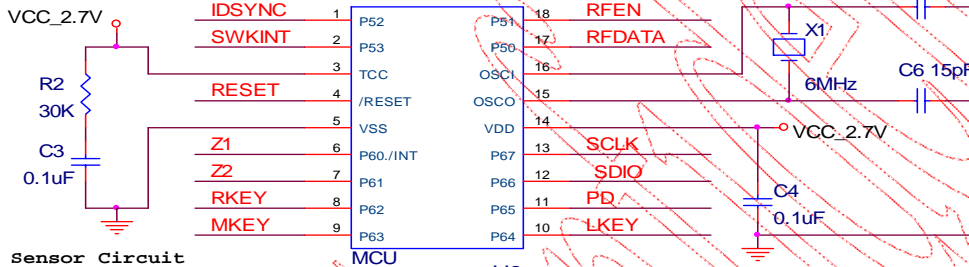
8.1 2.7V Application Circuit (with Red LED)

#1. Battery Power Circuit

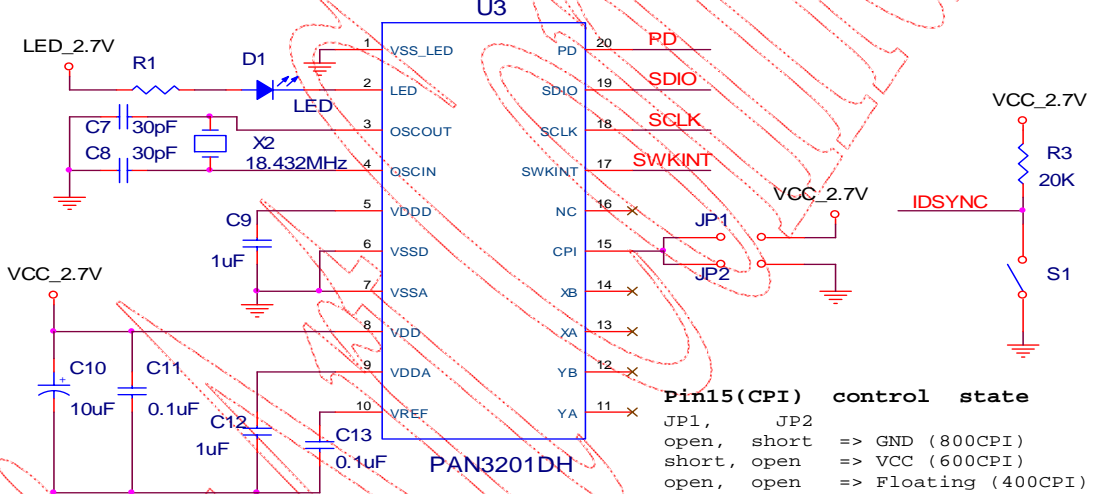
DC/DC Converter



#2. MCU Circuit



#3. Sensor Circuit



#4. RF TX Circuit

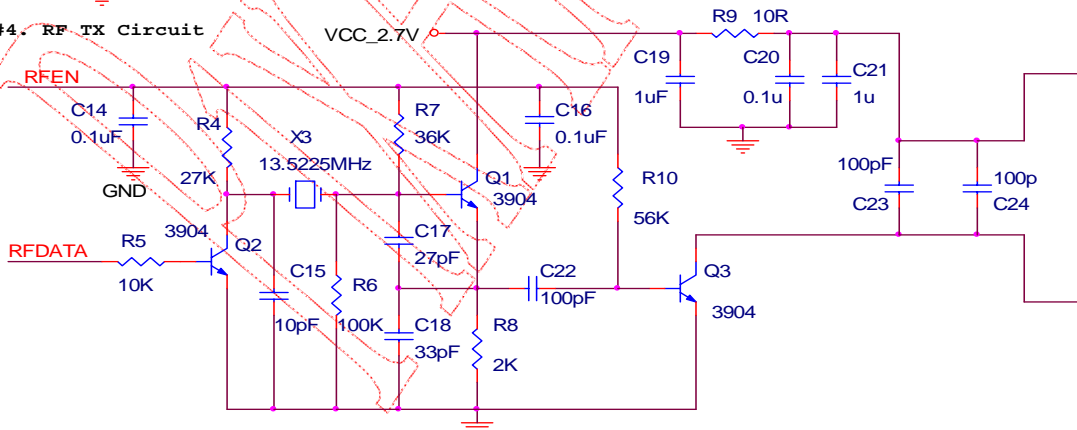


Figure14. Application Circuit for 2.7V (with Red LED)

8.2 1.8V Application Circuit (with Red LED)

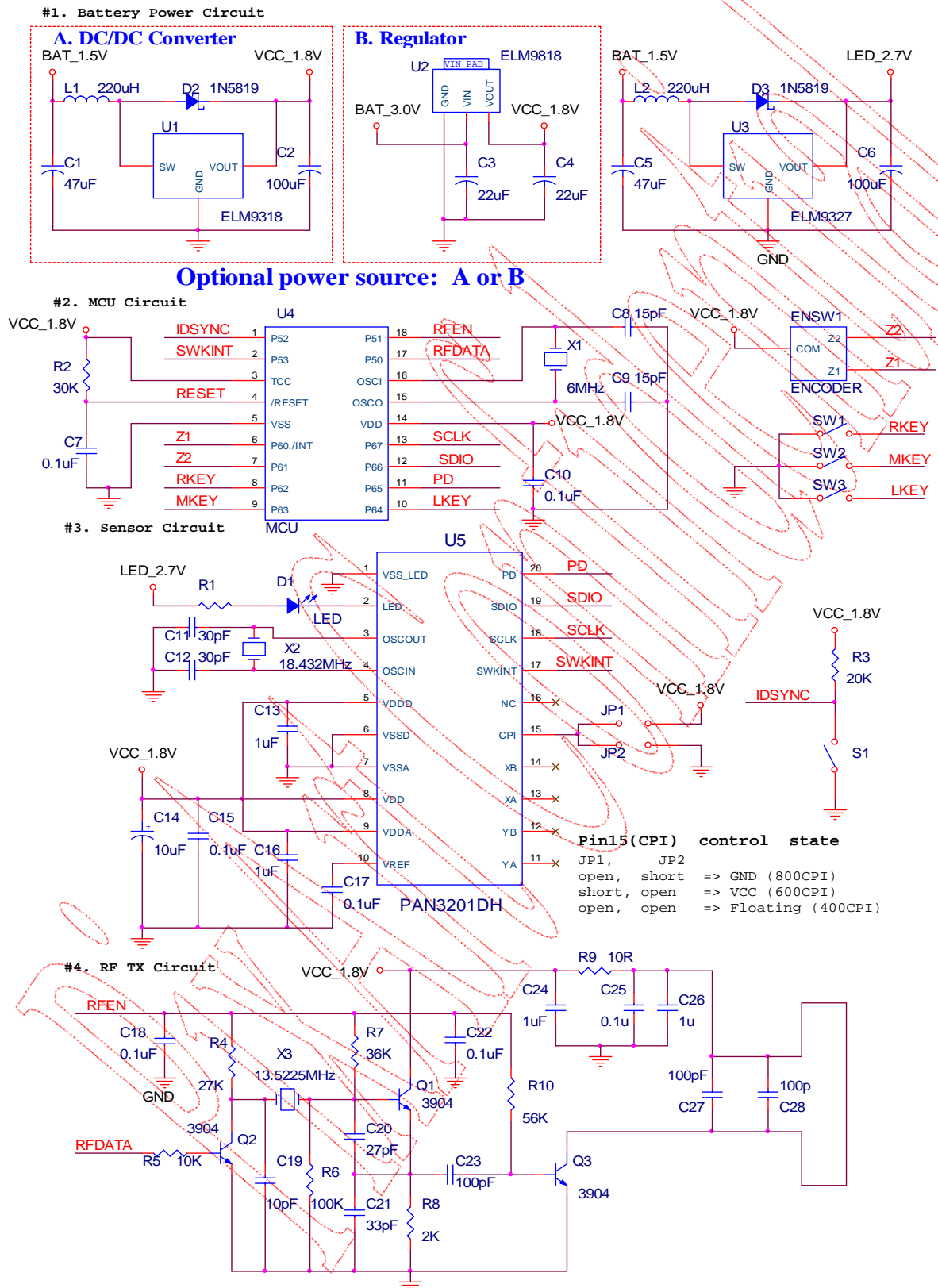


Figure15. Application Circuit for 1.8V (with Red LED)

8.3 1.8V Application Circuit (with IR LED)

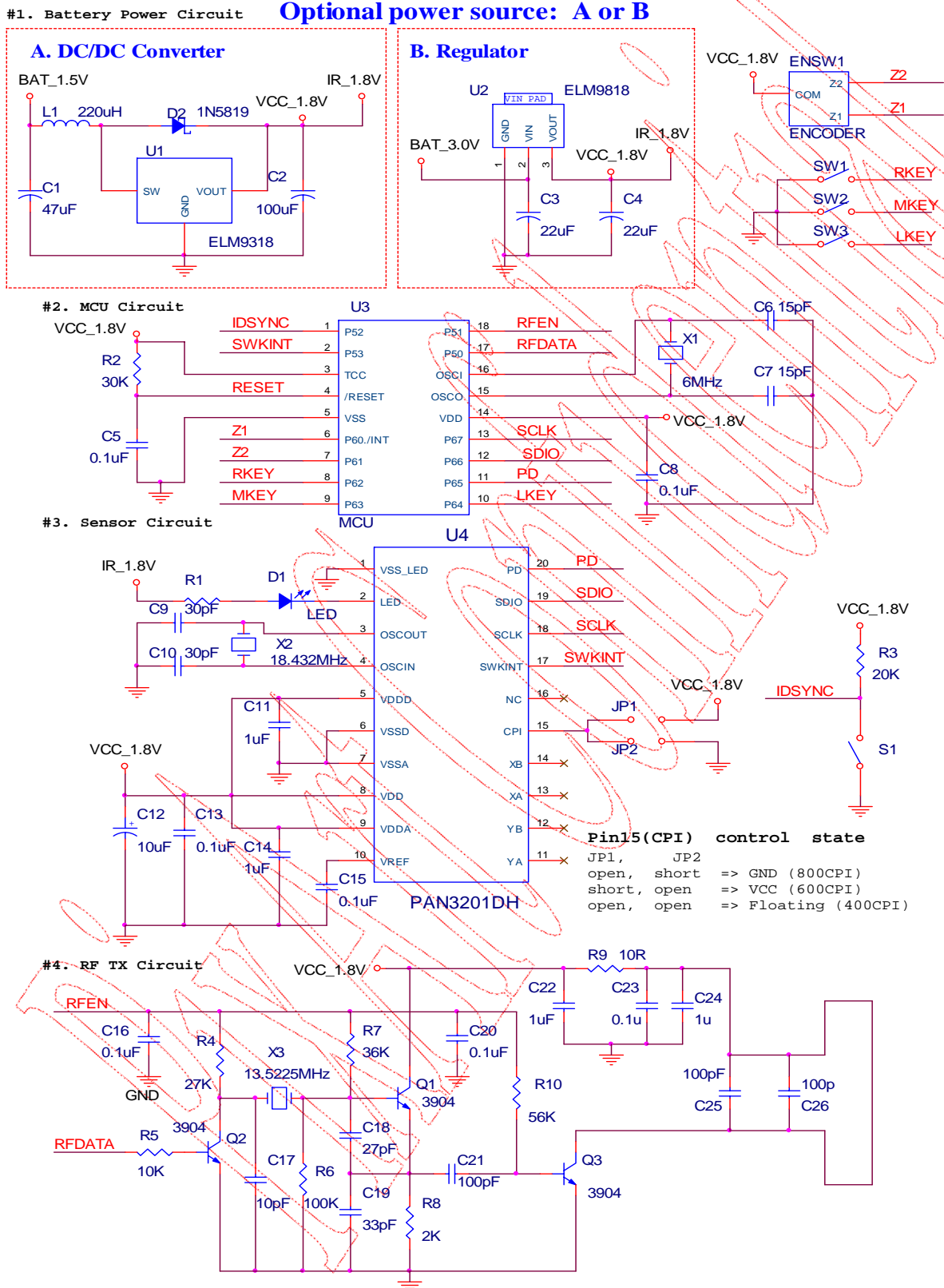


Figure16. Application Circuit for 1.8V (with IR LED)

8.4 Typical Application for RF Receiver

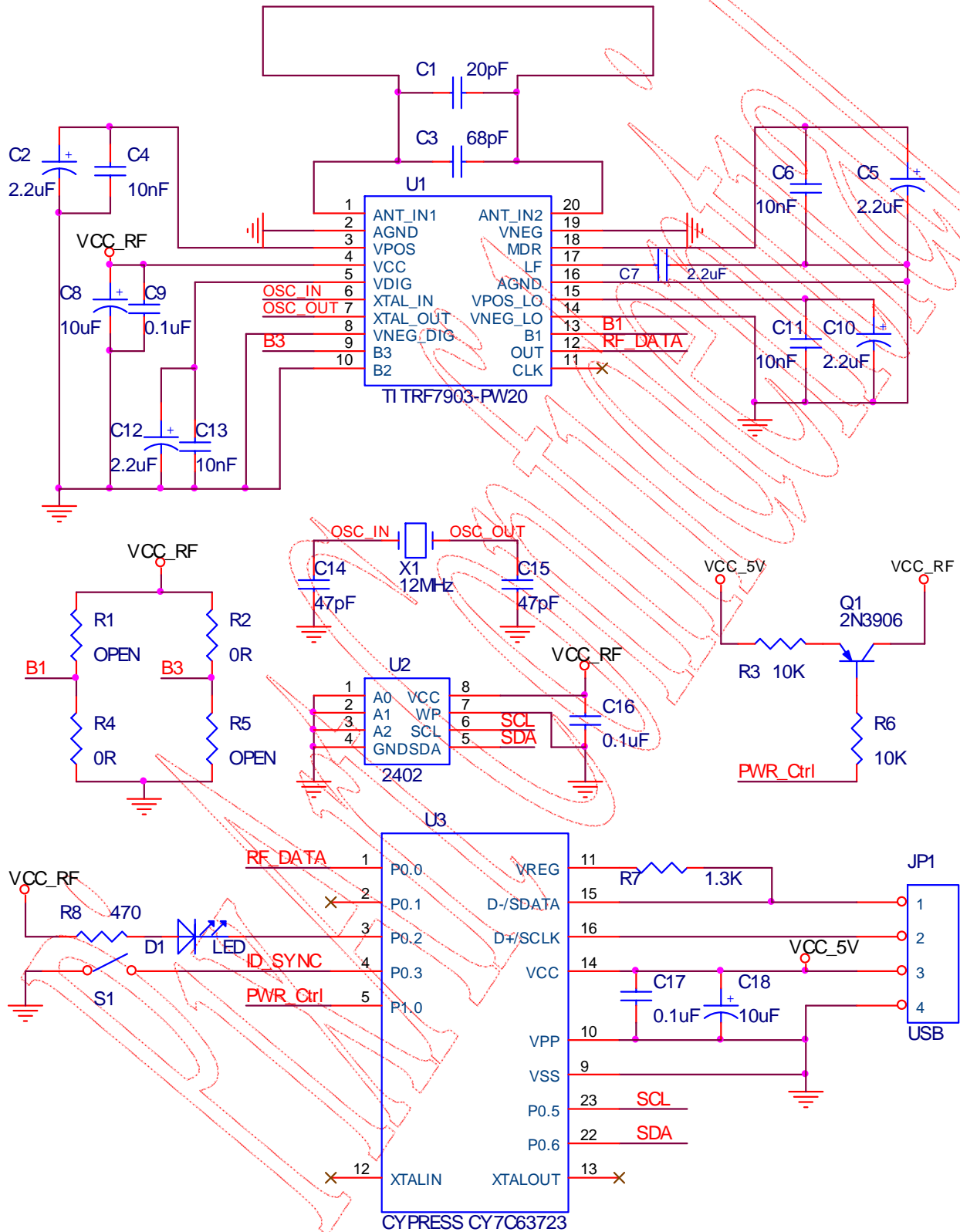


Figure17. Application circuit for RF Receive

8.5 PCB Layout Consideration

1. Caps for pins 5, 8, 9, 10 **MUST** have trace lengths **LESS** than **5mm**.
2. The trace lengths of OSCOUT, OSCIN must less than **6mm**.

8.6 Recommended Value for R1

8.6.1 Using Red LED

Radiometric intensity of red LED

Bin limits (mW/Sr at 20mA)

LED Bin Grade	Min.	Typ.	Max.
N	14.7	-	17.7
P	17.7	-	21.2
Q	21.2	-	25.4

Note: Tolerance for each bin will be $\pm 15\%$

Suggested R1:

Red LED Bin Grade	Suggested R1 (ohm)
N	12
P	12
Q	12

8.6.2 Using IR LED

Suggested R1:

IR LED Bin Grade	Suggested R1 (ohm)
TBD	0

It is not guaranteed that the performance of PAN3201DH with IR LED is as good as PAN3201DH with red LED. PAN3201DH is designed to a very good match with red LED, and this combination has the best performance.

8.6.3 Summary

Light Source	LED Bin Grade	VDD	R1 (ohm)
Red LED	N, P, Q	2.7	12
IR LED	TBD	1.8	0

9. Package Information

9.1 Package Outline Drawing

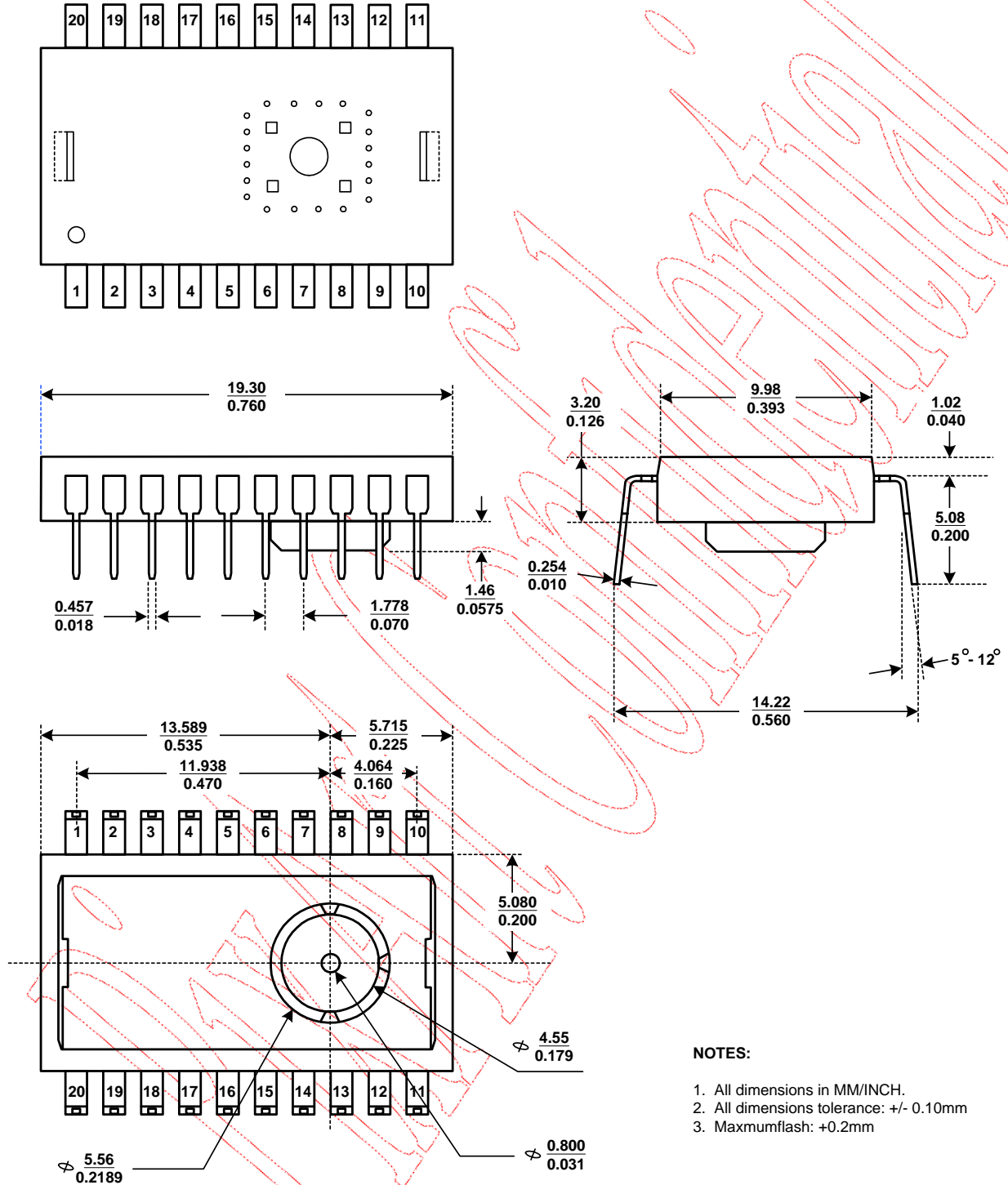


Figure 18. Package outline drawing

9.2 Recommended PCB Mechanical Cutouts and Spacing

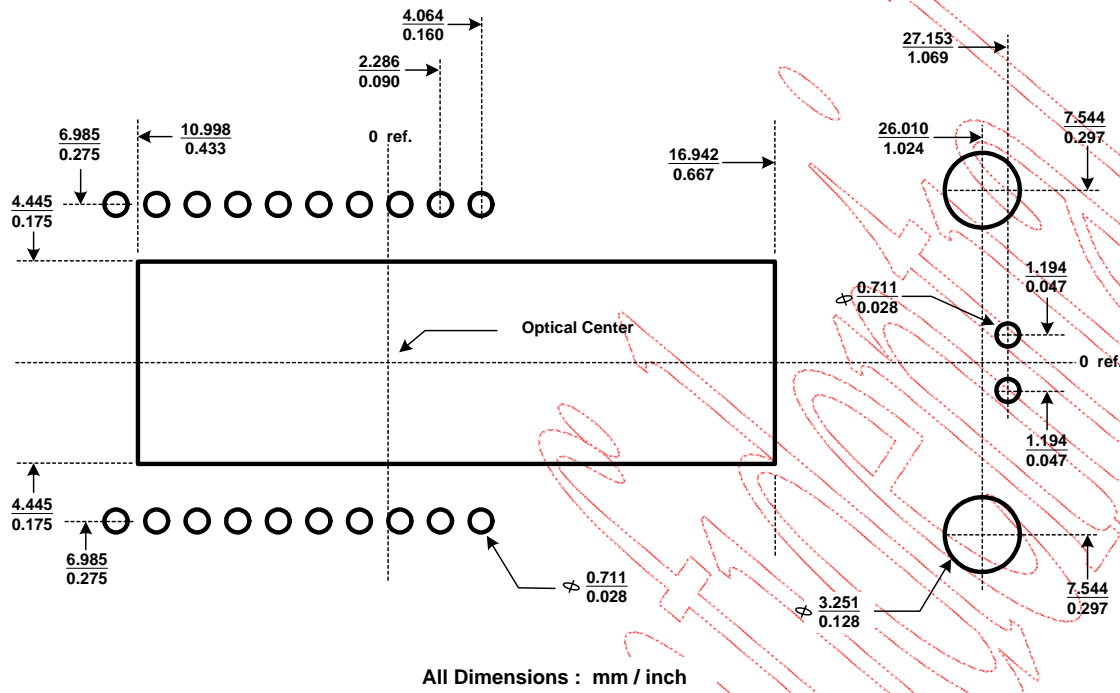


Figure 19. Recommended PCB mechanical cutouts and spacing

10. Update History

Version	Update	Date
V1.0	Creation, Preliminary 1 st version	03/02/2006